



PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Restructure OCuLink Power Specification Appendices ECR [R1.1]
DATE:	April 6, 2018
AFFECTED DOCUMENT:	OCuLink 1.0
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Part I

1. Summary of the Functional Changes

The contents of Appendices C and E which address power requirements for the optional external OCuLink cables has been restructured, including their titles, to clarify their contents.

1. Appendix C. External Cable Power Requirements.

- a. Title revised to: Requirements for Optional Peripheral Power in External Cables
- b. Appendix restructured into 4 sections: Power Source, Hot Plug, Power Sequencing, and Power Decoupling ~~plus the Power Requirements Table and the Peak Current Figure~~
- c. All content now addresses only the requirements for optional peripheral power in external cables.

2. Appendix E. Active Cable Assemblies

- a. Title revised to: Requirements for Optional Peripheral Active Cables Assemblies.
- b. Appendix restructured in a more orderly fashion for reader usability
- c. All content now addresses on the requirements for optional peripheral active cable assemblies.
- d. The paragraph addressing the use of SMBus has been clarified

2. Benefits as a Result of the Changes

The original content of Appendices C and E appeared to be intertwined which was confusing to the reader. The restructuring makes it clear that they are separate which supports the intent of the specification.

3. Assessment of the Impact

The ECN provides clarifications for requirements that affect both systems implementers and cable assembly suppliers. The revisions will save time and confusion for the implementation of the optional external OCuLink cables.

4. Analysis of the Hardware Implications

Minimal if any- interest for OCuLink has been internal to date.

5. Analysis of the Software Implications

N/A

6. Analysis of the C&I Test Implications

N/A

Part II

Change Appendix C as follows (see next page):



Appendix C – ~~External Cable Power~~ Requirements for Optional Peripheral Power in External Cables

C.1. Power Source

The requirements when implemented are:

- ☐ Optional ~~p~~Peripheral ~~P~~power shall only come from the ~~root~~Upstream Subsystem.
- ☐ Optional peripheral power~~only~~ supports up to ~~5~~10 W MAX on each of the two 5 V pins, totaling 10 W MAX per cable assembly,~~equally divided on the two 5-V pins.~~
- ☐ ~~Root devices~~Substream subsystems that provide optional peripheral power are responsible for preventing reverse current flow.
- ☐ In a ~~tethered configuration situation~~ where peripheral ~~5-V~~ power is supplied by the ~~Root~~Upstream Subsystem, V_{act} generated at the ~~end point~~Downstream Subsystem is included in the Upstream Subsystem's ~~root~~ 10 W total supply budget. Refer to Appendix E for V_{act} power requirements.
 - ☐ Peripheral power in all power management states is governed by the *PCI Express Base Specification*. Please refer to the Power Management chapter in the *PCI Express Base Specification*.
- ☐ ~~All OCuLink enclosures must support V_{act} (1.5 W Max per defined pins).~~
 - ☐ ~~V_{act} must be provisioned per connector end.~~
(i.e., V_{act} is not carried through the cable from the root to the end point).
 - ☐ ~~V_{act} must remain “on” in all power management states.~~
 - ☐ ~~Required to support cable management services.~~

~~To avoid exceeding system power supply limits and cooling capacity, all cables at power up, by default, must operate with ≤ 1.5 W. The maximum power level is allowed to exceed the classified power level for 500 ms, following hot insertion or power up. However, the current is limited to values given by Table C-1 and illustrated in Figure C-1.~~

~~At host power up the host must supply 3.3 V_{act} TX and 3.3 V_{act} RX to the cables within 100 ms of each other. Table C-1-1 is swept from 10 Hz to 10 MHz, according to the methods of C.3.3. This emulates the worst case noise of the host.~~

~~It is also desirable for a cable and host to each tolerate a degree of random or semi-random noise on both 3.3 Vact TX and 3.3 Vact RX, simultaneously, but the characteristics of this noise are beyond the scope of this document.~~

C.2. Hot Plug/ Removal (Surprise Insertion/ Removal)

- ☐ [The external OCuLink systems interface must detect cable presence prior to enabling any cable function including power from the connected cable.](#)
- ☐ [The system is responsible for safe-guarding against transient power such that it does not damage electrical components at either end. See the “AC Electrical Characteristics” section of SFF-8449 for more information.](#)
- ☐ [Refer to Table 6-11 for connector contact power ratings.](#)

C.3. Power Sequencing

[There is no specific requirement for power supply sequencing of each of the two 5V power supply wires. They are permitted to come up or go down in any order. The Upstream Subsystem, however, must assert the PERST# signal if either of the two 5V power wires go outside of the specification.](#)

C.4. Power Decoupling

[Due to the low level signaling of the PCI Express interface, it is strongly recommended that sufficient decoupling of all power supplies be provided \(see SFF-8449 “Power Supply Filtering Network” for recommended filter design\). This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote Upstream PCI Express device.](#)

- ☐ [The external OCuLink interface must meet applicable safety standards. Usually this means that a powered connection implements current limiting on any devices connected to the interface. Two examples are:
 - \[Active cables\]\(#\)
 - \[Power delivery to Downstream Subsystem ports\]\(#\)](#)

~~Table C-1. OCuLink Cable Assembly Power Requirements~~

Parameters	Symbol	Conditions	Min	Max	Units
Power supply noise tolerance including ripple {peak-to-peak}	-		-	66	mV
Power supply voltages including ripple, droop and noise below 100 kHz	3.3 V_{act} TX 3.3 V_{act} RX	Note 1	3.14	3.46	V
Instantaneous peak current at Hot-Plug	-	Note 2, 3	-	400	mA
Sustained peak current at Hot-Plug	-	Note 2, 3, 5	-	330	mA
Instantaneous peak current on enabling	-	Note 2, 3, 5	-	600	mA
Sustained peak current on enabling	-	Note 2, 3, 5	-	500	mA
Maximum power consumption	-	Note 4	-	1.5	W
Maximum power consumption at power up		Note 4		1.5	W

Notes:—

- ~~1. Set point is measured at the input to the connector on the host board reference to ground. Droop is any temporary drop in voltage of the power supply, such as that caused by plugging in another cable assembly or when enabling another cable assembly.~~
- ~~2. The requirements for current apply to the current through each inductor.~~
- ~~3. The maximum currents are the allowed currents for each power supply; therefore, the total module peak currents are permitted to be twice this value. The instantaneous peak current is allowed to exceed the specified maximum current capacity of the connector contact for a short period, see Figure C-1.~~
- ~~4. Maximum cable assembly power consumption must not exceed 1.5 W from 500 ms after power up.~~
- ~~5. Not to exceed the sustained peak limit for more than 50 us; but is permitted to exceed this limit for shorter durations.~~

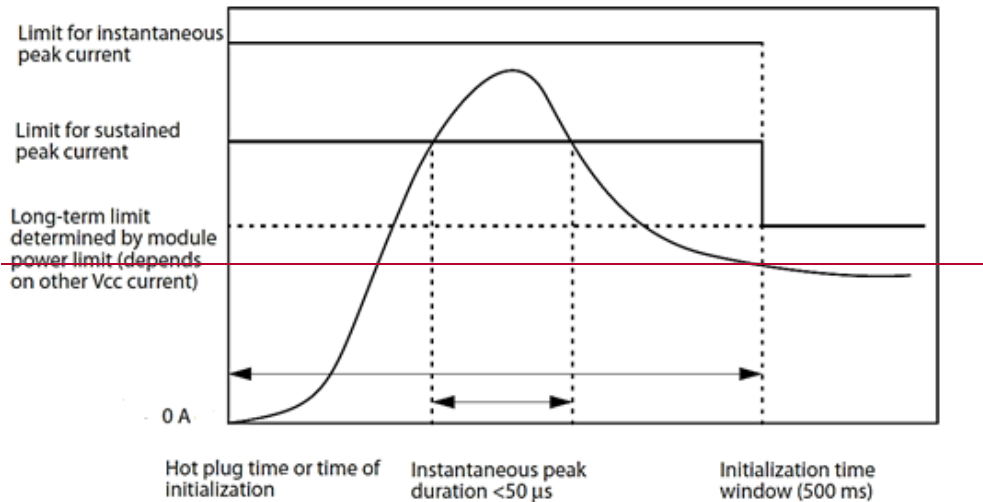


Figure C 1. Instantaneous and Sustained Peak Current for 3.3 Vact TX and 3.3 Vact RX

C.1. Power Sequencing

There is no specific requirement for power supply sequencing of each of the two power supply rails. They are permitted to come up or go down in any order. The system, however, must assert the PERST# signal whenever either of the two power rails go outside of the specifications.

C.2. Power Decoupling

Due to the low level signaling of the PCI Express interface, it is strongly recommended that sufficient decoupling of all power supplies be provided. This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote Upstream PCI Express device.

Change Appendix E as follows (see next page):



Appendix E — Requirements for Optional Peripheral Active Cable Assemblies

- ☐ External Host Board-side Cable interfaces intended to operate at PCIe Gen 3 (8.0 GT/s) must be designed to support both passive and active cables.
- ☐ All OCuLink enclosures must support 3.3 V_{act} (1.5W MAX per defined pins).
- ☐ Active cables require both the Upstream Subsystem and Downstream to provide 3.3 V_{act} to their respective cable plugs. 3.3 V_{act} does not go down the cable therefore 3.3 V_{act} must be provisioned per connector end.
- ☐ At Subsystem power up and plug-in events, the Subsystem must supply 3.3 V_{act} TX and 3.3 V_{act} Rx to the cable within 100 ms of each other.
 - ☐ This refers to the energizing of the cable/ connector, and not to platform power on.
 - ☐ Peripheral power in all power management states is governed by the *PCI Express Base Specification*. Please refer to the Power Management chapter in the *PCI Express Base Specification*.
 - ☐ 3.3 V_{act} is required to support cable management services.
- ☐ Active cables must contain non-volatile memory.
- ☐ Each cable manufacturer is responsible for:
 - ☐ Creating and storing data in a method consistent with Appendix A and Appendix B.
 - ☐ Ensuring that the Link is able to operate when using the eye diagrams defined in the *PCI Express Base Specification*, and other ~~PCI Express Specifications listed in Section 1.1 Reference Documents~~ applicable specifications.
- ☐ Active cable behavior must take into account Link training protocol specified in the *PCI Express Base Specification*, and be able to accept the potential changes from the Subsystem Transmitters during Link training at 8.0 GT/s.
- ☐ Active cables must initially operate at 2.5 GT/s in order to ensure initial Link training and then operate at the highest Link speed supported.
- ☐ Active cables must ~~must~~ transparently support Electrical Idle and Receiver Detect.
- ☐ Active cables ~~Permitted are designed~~ to support arbitrarily long cable lengths as constrained by the active component power budget and PCI Express clocking schemes in specific applications.
- ☐ ~~Permitted to be visible to enclosure software as required for identification and management purposes.~~
- ☐ ~~Active cables require both the ROOT and ENDPOINT to provide 3.3 volts.~~
- ☐ ~~Only the ROOT supplies 5 volts to power endpoint (downstream) devices.~~

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- Active cables to be visible to enclosure software as required for identification and management purposes. The use of SMBus across the cable is an optional feature.
 - The SMBus/ 2-Wire interface employed in this specification can either be a Passive or Active implementation. The Passive solution may provide a 2-Wire connection from the Upstream Subsystem to the Downstream Subsystem to determine its usage or for device management.
 - ~~Due to complexity, Active Optical Cables may choose not to implement this option. This allows the use of cables that adhere to SFF-8449, for a PCI Express interface with a reduced feature set. Active Optical Cable assemblies may not want to implement SMBus across the cable for cost or complexity reasons, and therefore are permitted to have a reduced feature set. Requirements for PCI Express cables with reduced feature sets are described in SFF-8449. The Upstream Subsystems should not be designed in such a way as to require the use of SMBus across the cable. However, the SMBus controller is still required, by both Upstream and Downstream fixed ends, to read the cable assembly information for configuration of the PCIe devices that are part of the cabled Link.~~
 - It is the system implementer's responsibility to meet the electrical Specifications for the SMBus, when used across the cable.
- ~~The External OCuLink interface must be designed to meet applicable safety standards. Usually, this means that a powered connection implements current limiting on any devices connected to the interface. Two examples are:~~
 - ~~Active cables~~
- ~~Power delivery to Downstream endpoint ports.~~ Refer to Appendix C for information on external cables.